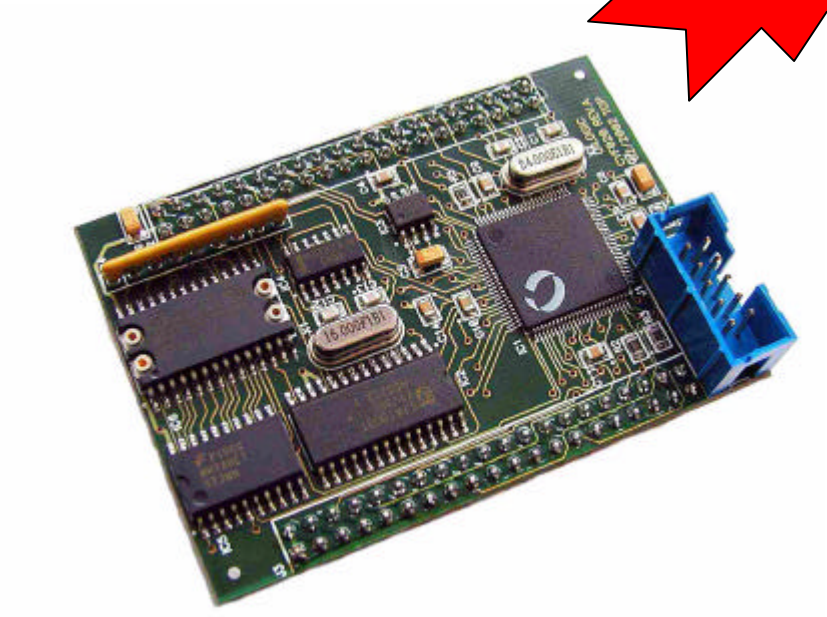
DILOGIC

CYF120

DATA SHEET

100MIPS !



CYF120

Single Board Computer, Sub-credit Card Size (68x48mm)
with Silicon Laboratories C8051F120 microcontroller.

Product specification — January,2004

CYF120 Leaflet — Version 1.1

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DESCRIPTION

The **CYF120** is a Single Board Computer based on the Silicon Laboratories (www.silabs.com) C8051F120 microcontroller. C8051F120 is highly advanced System-On-Chip (SoC), containing single-clock-cycle 8051 compatible core, running up to 100MHz with up to 100MIPS throughput. In addition, there is 128KB of FLASH memory, 8KB if internal SRAM memory, 8-input 12-bit 100ksps A/D converter, 8-input 8-bit 500ksps A/D converter , 2 12-bit D/A converters, 2 analog comparators, 2.4V reference, 2 UART's, SPI™ bus controller, SMS (I^2C™-compatible) bus controller, programmable counter array and 5 general purpose 16-bit timers. There's also 40-bit MAC for accelerating DSP algorithms. One of the unique features is the availability of non-intrusive **on-chip debug port via standard JTAG interface**, allowing also in-circuit FLASH programming !

Further information about C8051F120 is available from Silicon Laboratories web site (http://www.silabs.com/products/pdf/C8051F120Rev1_2.pdf).

CYF120 is a **6-layer** PCB module and contains, in addition to C8051F120, 32KB of battery-backed SRAM, RTC, and CAN-controller. All free C8051F120 port pins are brought to two 2x20 pin headers with standard raster (2,54mm/0,1"). This allows plug-in of the module to the target application PCB.

Development board is available for quick development start.

FEATURES

- SBC in Sub-credit Card size (68x48mm), SMD technology, 6-layer PCB for improved analog signal integrity
- Powerful Silicon Laboratories C8051F120 CPU running at up to 99.5MHz
- **On-chip JTAG debug port !!!**
- 128KB FLASH
- 16x16 hdw. multiplier with 40bit MAC for DSP
- 32KB battery-backed SRAM with replaceable Lithium battery pack
- RTC
- SJA1000 CAN 2.0 controller
- 12-bit ADC with 8 multiplexed inputs and programmable gain amplifier
- additional 8-bit ADC with 8 multiplexed inputs and programmable gain amplifier
- two voltage output 12-bit DAC's
- internal 2,4V reference voltage
- on-chip linear temperature sensor
- on-chip brown-out voltage detector
- on-chip watch-dog timer
- 2 full-duplex UART's
- SPI™-compatible serial interface
- SMS-bus serial interface (I^2C™ compatible)
- Requires single 5V/50mA power supply
- Comes with FLASH loader via serial port
- Operates within a standard 0 to 70°C range
- Extended temperature range available on request

BLOCK DIAGRAMS

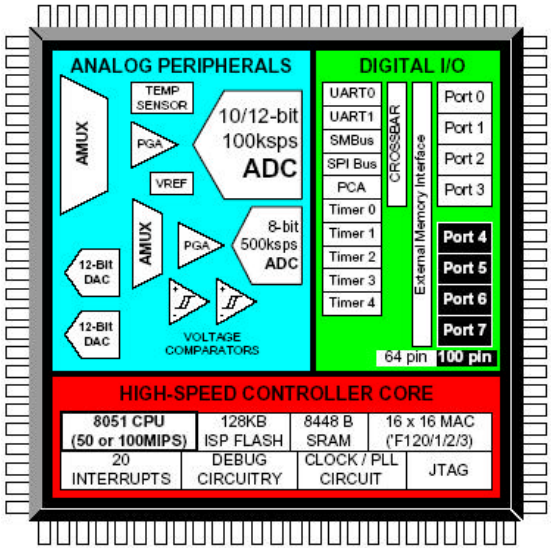

Fig.1 C8051F120 block diagram

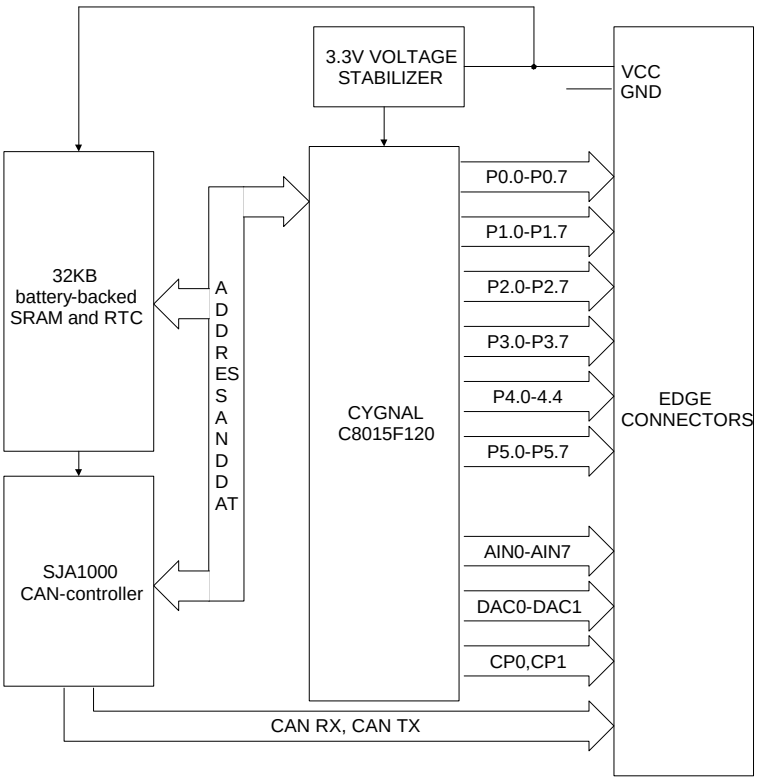

Fig.2 CYF120 block diagram

MEMORY MAP

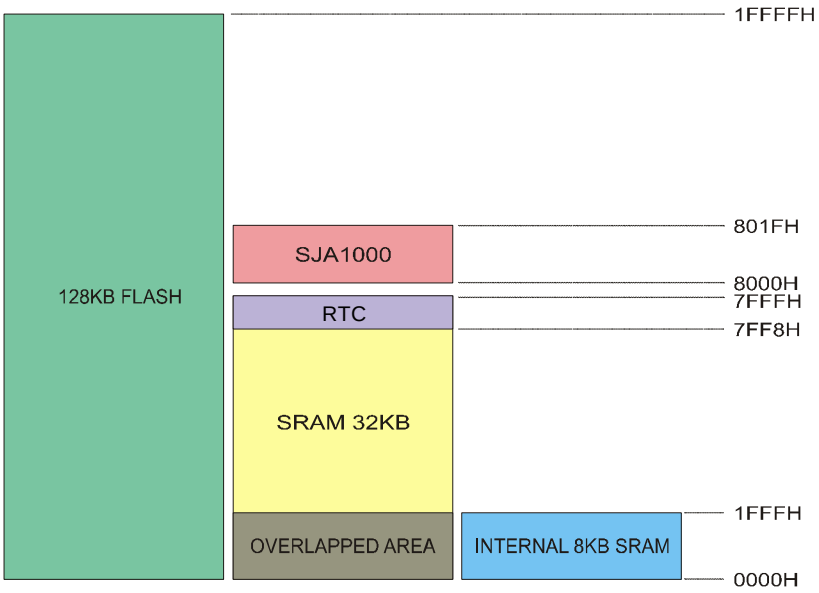

Fig.3 CYF120 memory map

TOP VIEW

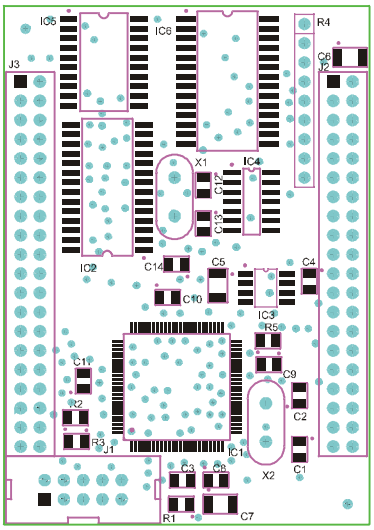

Fig.4 CYF120 top view

CONNECTOR PINOUT

Connector J2

Pin	Description
1.	VCC
2.	VCC
3.	GND
4.	GND
5.	P0.0
6.	P0.1
7.	P0.2
8.	P0.3
9.	P0.4
10.	P0.5
11.	P0.6
12.	P0.7
13.	P3.0
14.	P3.1
15.	P3.2
16.	P3.3
17.	P3.4
18.	P3.5
19.	P3.6
20.	P3.7
21.	P2.0
22.	P2.1
23.	P2.2
24.	P2.3
25.	P2.4
26.	P2.5
27.	P2.6
28.	P2.7
29.	P1.0
30.	P1.1
31.	P1.2
32.	P1.3
33.	P1.4
34.	P1.5
35.	P1.6
36.	P1.7
37.	CANTX0
38.	CANTX1
39.	CANRX0
40.	CANRX1

Connector J3

Pin	Description
1.	VCC
2.	VCC
3.	GND
4.	GND
5.	P5.7
6.	P5.6
7.	P5.5
8.	P5.4
9.	P5.3
10.	P5.2
11.	P5.1
12.	P5.0
13.	P4.4
14.	P4.3
15.	P4.2
16.	P4.1
17.	P4.0
18.	/RESET
19.	AGND
20.	AGND
21.	VREF
22.	/CANIRQ
23.	CP0+
24.	CP1+
25.	CP0-
26.	CP1-
27.	DAC0
28.	DAC1
29.	AIN0
30.	AIN1
31.	AIN2
32.	AIN3
33.	AIN4
34.	AIN5
35.	AIN6
36.	AIN7
37.	AGND
38.	AGND
39.	Reserved
40.	Reserved

NOTE:

AGND is connected to GND via 2.2 Ohm resistor!

http://www.dilogic.hr

DISCLAIMER:

DILOGIC reserve the right to make changes, without notice, in the products, or/and software, described or contained herein in order to improve design or/and performance. DILOGIC assumes no responsibility or liability for the use of any of these products.

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